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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/084,466	02/28/2002	Hiroyuki Matsumoto	ASAM.0041	4986

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EXAMINER	
NGUYEN, LUONG TRUNG	
ART UNIT	**PAPER NUMBER**
2612	

DATE MAILED: 08/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/084,466	MATSUMOTO ET AL.	
	Examiner	Art Unit	
	LUONG T. NGUYEN	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7-11* is/are rejected.

7)☒ Claim(s) *6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/28/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Objections

2. Claim 6 is objected to because of the following informalities:

Claim 6, line 9, "a program" should be changed to --the program--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Poplin et al. (U. S. Patent Application No. 2004/0201729).

Regarding claim 1, Poplin et al. discloses an imaging system including a solid-state CMOS imaging device (CMOS array 10, Figures 1-2, Page 3, Sections [0026], [0027]) and a signal processing semiconductor integrated circuit for processing read-out signals of pixels from

said solid-state CMOS imaging device (image processing circuitry 22 and flicker detector 24, Figure 1, Page 3, Sections [0026], [0027]), wherein said signal processing semiconductor integrated circuit is configured to be able to identify a frequency of a light source illuminating an object to be imaged on the basis of the read-out signals of the pixels from said solid-state CMOS imaging device without using a photoelectric conversion element dedicated to detect alight amount of the light source (flicker detector 24 determines the periodicity of the lighting fluctuation (frequency of a light source), Figure 1, Page 3, Sections [0026], [0027]).

5. Claims 2-5 are rejected under 35 U.S.C. 102(e) as being anticipated by Kasahara et al. (U. S. Patent No. 6,710,818).

Regarding claim 2, Kasahara et al. discloses an imaging system including a solid-state CMOS imaging device and a signal processing semiconductor integrated circuit for processing read-out signals of pixels from said solid-state CMOS imaging device, comprising:

first level detection means for detecting brightness on a first area (a horizontal line) set up on an imaging area of said solid-state CMOS imaging device (the flicker judging circuit 5 judges whether illumination flicker exist in the video signal by frequency analyzing the dividing results of horizontal lines, Column 8, Lines 5-32, Column 2, Lines 30-55).

second level detection means for detecting brightness on a second area larger (a plurality of horizontal lines) than first area (the flicker judging circuit 5 judges whether illumination flicker exist in the video signal by frequency analyzing the dividing results of horizontal lines, Column 8, Lines 5-32, Column 2, Lines 30-55).

judgment means for judging turning-on-and-off of a light source illuminating (judging flicker) an object to be imaged on the basis of detection levels of said first and second level detection means (the flicker judging circuit 5 judges whether illumination flicker exist in the video signal by frequency analyzing the dividing results of horizontal lines, Column 8, Lines 5-32, Column 2, Lines 30-55).

Regarding claim 3, Kasahara et al. discloses wherein said judgment means judges that said light source illuminating the object is turned on and off when variation in the detection level of said first level detection means is large and variation in the detection level of said second level detection means is small (Column 9, Lines 50-67).

Regarding claim 4, Kasahara et al. discloses wherein said first area is constituted by pixels on a single horizontal scanning line (said unit area is a horizontal line, Column 2, Lines 50-55) and said second area is constituted by pixels on a plurality of horizontal scanning lines (said unit area is a plurality of horizontal lines, Column 2, Lines 50-55).

Regarding claim 5, Kasahara et al. discloses charge storage control means for setting up an electric charge storage time for each pixel of said solid-state CMO imaging device to be equal to a turning-on-and-off period of said light source illuminating the object or an integral multiple thereof to thereby remove flicker (compensating flicker, Column 1, Lines 14-18, Column 2, Line 38-55).

6. Claims 7-9, 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Oda et al. (U. S. Patent No. 6,882,363).

Regarding claim 7, Oda et al. discloses an imaging system using a solid-state CMOS imaging device (MOS type imager 1, Figure 1, Column 3, Line 62 – Column 4, Line 18), comprising charge storage control means for setting up an electric charge storage time for each pixel to be equal to turning-on-and-off period of a light source illuminating an object to be imaged or an integral multiple thereof (in order to prevent flicker, the electronic shutter speed is set to be an integer times the luminance average level variation period of fluorescent lamps within the storing cycle, Figure 1, Column 3, Line 62 – Column 4, Line 18).

Regarding claim 8, Oda et al. discloses wherein charge storage control means sets up said electric charge storage time while using, as a unit, time required to scan a single horizontal scanning line (Column 1, Lines 31-40).

Regarding claim 9, Oda et al. discloses wherein charge storage control means change over said charge storage time in response to said turning-on-and-off period of said light source illuminating the object or an integral multiple thereof to set up an electric charge storage amount for each pixel variably stepwise and interpolates differences in stored light amounts between steps by means of continuous gain control of read-out signals of pixels (the shutter interval of the imager is changed stepwise, Column 3, Lines 5-60).

Regarding claim 11, Oda et al. discloses wherein said gain control is performed to the read-out signals of pixels taken out outside of said solid-state CMOS imaging device (automatic gain control circuit 2 is outside imager 1, Figure 1).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Oda et al. (U. S. Patent No. 6,882,363) in view of Muramatsu et al. (U. S. Patent No. 6,900,837).

Regarding claim 10, Oda et al. fails to specifically disclose wherein said gain control is performed within said solid-state CMOS imaging device. However, Muramatsu et al. teaches a camera system 100 used MOS type image sensor (CMOS imaging device), which gain control GCA 2 is performed within camera system 100 (Figure 4). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device in Oda et al. by the teaching of Muramatsu et al. in order to provide a compact system, which reduces space for circuitry.

Allowable Subject Matter

9. Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Chung et al. (U. S. Patent No. 6,271,884) discloses image flicker reduction with fluorescent lighting.

Toyoda et al. (U. S. Patent No. 6,630,953) discloses flicker control imaging apparatus.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to LUONG T. NGUYEN whose telephone number is (571) 272-7315. The examiner can normally be reached on 7:30AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, WENDY GARBER can be reached on (571) 272-7308. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LN
08/22/05

LUONG T. NGUYEN
PATENT EXAMINER